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High Performance DCT Implementation Using Reduced Complexity Wallace Multiplier and High Speed Carry Select Adder

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Abstract: Discrete cosine Transform are widely used in video and image compression standards. This paper focuses on the implementation of Discrete Cosine Transform DCT) using reduced complexity Wallace multiplier and high speed carry select adder. Wallace Multipliers basically use full adders and half adders in their reduction phase. The number of partial product bits are not being reduced by the half adder. Therefore minimizing the number of half adders in the multiplier will reduce the complexity. In the modified Wallace tree number of half adders are reduced to 80 percent. Inorder to improve the speed a carry select adder with D Latch is being used in the final carry propagation path. The design entry is done in Verilog and simulated using ModelSim 6.1.

Key Words: BEC, Wallace, Modified Wallace, CSA

I. INTRODUCTION

Many application today use digital signal processing in a wide variety of areas due to the increasing advances in technology. Multimedia applications, for examples, use algorithms to code video and images to reduce large amount compression to de correlate the signal and increase the compression efficiency. DCT is a complex operation and uses significant amount of computing resources [1-3].

Due to the use of multipliers, a significant amount of power and computations are required in DCT. The well known Wallace high speed multipliers uses carry save adders to reduce an N-row bit product matrix to an equivalent two row matrix that is then summed with carry propagation adder to give the product[4]. In this work some modification is performed in the structure of Wallace Tree multiplier in order to reduce the complexity and thereby the power consumption. Wallace multipliers consist of three stages of computation. In the first stage, partial product matrix is formed. In the second stage, partial product matrix is reduced to a height of two. In the final stage, these two rows of partial products are combined using carry propagation adder.

This paper is concerned with the second phase where the N rows of partial product bits are reduced to two rows. The Wallace approach uses several stages of full and half adders as carry save adders that are arranged to maximize the reduction at each stage. Full adders take in three bits and output two bits for a net reduction of one bit per full adder. Half adders take in two bits and output two bits. So there is no bit reduction occurs in half adders. In this work the number of half adders is reduced to 80%.

For the final carry propagation adder we use Carry select adder. Carry select adder having Binary to Excess one converter in its basic structure is available. But it offer some speed penalty. This disadvantage can be overcome by using D Latch instead of BEC

II. WALLACE MULTIPLIER

For the conventional Wallace reduction method, once the partial product array is formed, adjacent rows are collected into non overlapping groups of three. Each group of three rows are reduced by 1) applying a full adder to each column that contain three bits, 2) applying a half adder to each column that contain two bits 3) passing single bit column to the next stage without processing. This reduction method is applied to each stage until two rows remaining.

The final two rows are summed using a carry propagating adder. Since the Conventional Wallace multiplier perform the reduction as soon as possible more number of full adders and half adders are required. So the device utilization and the power consumption is more in Conventional Wallace Multiplier. Conventional Wallace Multiplier for N=8 is shown in figure 1.

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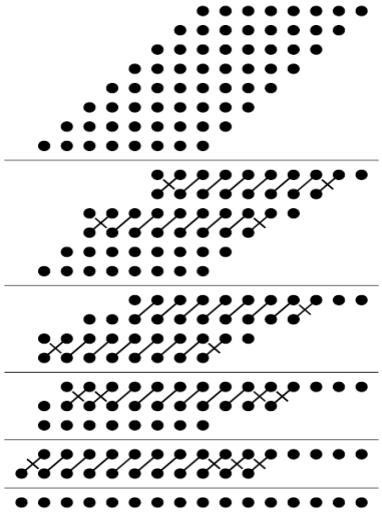

Fig 1. Wallace Multiplier for N=8

III. MODIFIED WALLACE MULTIPLIER

The Modified Wallace multiplier is similar to that of Conventional Wallace multiplier in that it uses as many full adders as possible, but different in that it only use half adders when necessary to ensure that the number of reduction stage is same as for Conventional Wallace Tree multiplier[5].

The Modified Wallace Tree at first make the partial product formed into the pyramidal structure and divide the structure into group of rows depending on the number of bits to be multiplied and uses full adders for each group of three bits in a column. A group of two bits in a column is not processed, that is, it is passed on to the next stage and there by reducing the number of half adders required. Single bits are passed on to the next stage as in the conventional Wallace reduction. Modified Wallace Multiplier for N=8 is shown in figure 2.

The only time the half adders are used to ensure that the number of stages of the modified Wallace multiplier does not exceed that of the conventional Wallace multiplier. For some cases the half adders are used only in the final stage of reduction.

The modified Wallace reduces the number of half adders required at least 80 percent compared to the conventional Wallace reduction with a slight increase in the number of full adders.

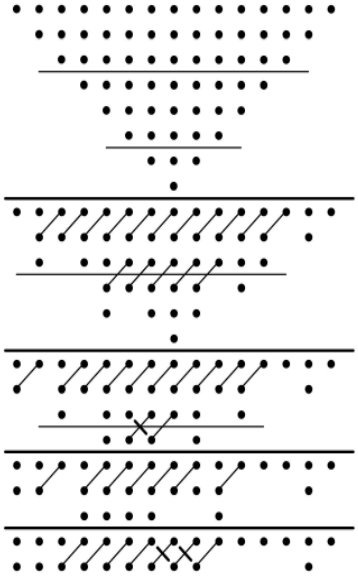

Fig 2. Modified Wallace Multiplier for N=8

IV. CARRY PROPAGATION ADDER

1. Carry Select Adder using D Latch

In the previous works hybrid adders are used for the final carry propagation part. The hybrid adders consist of carry look ahead adder and carry select adder. But carry select adder takes more area. So carry select adder which include BEC (Binary to Excess One converter) in its structure is included[6,7]. But it offers some speed penalty. In this structure the RCA with carry input equal to one is replaced by BEC. The structure of BEC for five inputs is given in figure 3.

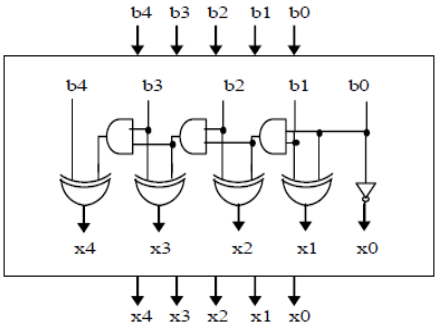

Fig 3. 5 bit Binary to Excess One Converter

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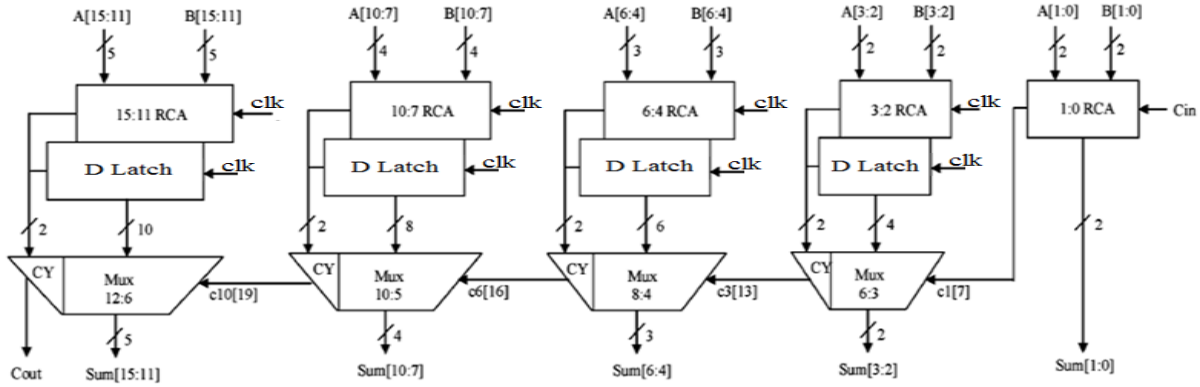

Fig 4. Carry Select Adder using D Latch

In the proposed architecture the BEC is replaced by D Latch which avoids the speed penalty introduced by BEC. In BEC the sum and carry for Cin=1 is calculated only after the sum and carry for Cin=0 is calculated. In the carry select adder structure using D Latch the sum and carry for cin=0 and cin=1 is calculated within the one clock cycle itself. So the speed penalty introduced by Carry Select Adder using D Latch can be avoided. The basic structure of carry select adder using D Latch for 16 bits is shown in figure 4.

This is a 16-bit adder in which least significant bit adder(LSB) is a ripple carry adder, which is two bit wide. The upper half of the adder is 14 bit wide which work according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in the adder itself. The latch is used to store sum and carry for cin=1. The carry out from the previous stage is used as control signal for multiplexer to select final output carry and sum. Cout is the final output carry. Figure 5 shows the internal structure of group 2 of the proposed 16 bit carry select adder. The group 2 performed the two bit addition which are a2 with b2 and a3 with b3. This is done by two full adders named FA2 and FA3 respectively. The third input to the full adder FA2 is clock instead of carry and third input to the full adder FA3 is the carry output from the FA2. The group 2 structure has three D Latches in which two are used for storing the su2 and sum3 from FA2 and FA3 and the last one is used to store carry. Multiplexer is used for selecting sum and carry according to the carry from the previous stage.

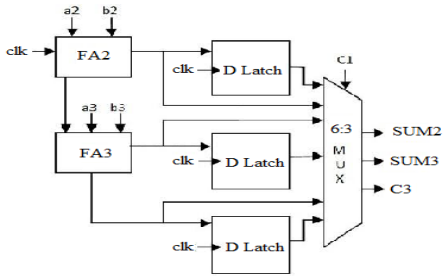

Fig 5. Group 2

V. DCT IMPLEMENTATION

A one dimensional N point DCT of a given data X can be given by

$$X(K) = e(k) \sum_{n=0}^{N-1} x(n) \cos\left[\pi \frac{(2n+1)k}{2N}\right] \ldots\ldots\ldots(1)$$

where

K=0,1,…N-1

Discrete Cosine Transform are important to numerous applications in science and engineering. The algorithm-architecture transformations can be used to derive efficient DCT implementations. The structure of constant geometry DCT algorithm is shown in figure 6. In this structure the multipliers used is Wallace multipliers. By using modified Wallace multiplier instead of Wallace multiplier the power and device utilization can be reduced. By introducing carry select adder with D Latch in the final Carry propagation path the speed can be improved.

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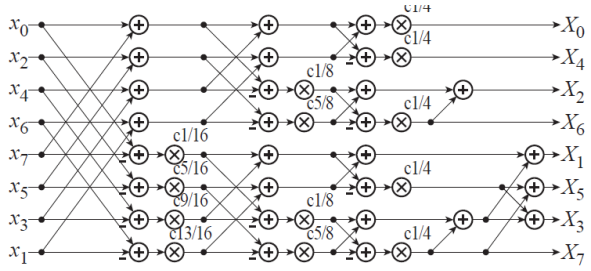

Fig 6. DCT structure

VI. SIMULATION RESULTS

The number of full adders and half adders required for Wallace and Modified Wallace multiplier is shown in Table I

TABLE I
COMPLEXITY OF THE REDUCTION

Input size	8	16	32	64
WALLACE				
FA	38	200	906	3850
HA	15	52	156	430
TOTAL GATES	402	2008	8788	36388
MOD WALLACE				
FA	39	201	907	3853
HA	3	9	23	53
TOTAL GATES	363	1845	8263	34889

The comparison result of Wallace and Modified Wallace multiplier using carry select adder using BEC and carry select adder using D Latch in the final carry propagation part is shown in Table 2.

TABLE II. COMPARISON RESULTS OF MULTIPLIERS

Multiplier	Bit	Devices		Delay(ns)	
		BEC	D Latch	BEC	D Latch
WALACE	8bit	162	208	31.8	26.1
	16bit	646	679	54.5	46.3
	32bit	1291	1391	72.8	63.3
MOD WAL	8bit	143	143	27.4	26.0
	16bit	567	567	52.6	49.8
	32bit	1118	1136	70.7	64.8

By using carry select adder using D Latch in the final carry propagation path instead of carry select adder with BEC the speed can be increased. The various parameter for CSA using BEC and using D Latch is shown in Table III.

TABLE III
COMPARISON RESULT FOR ADDERS

Parameters	CSA using BEC(16 bits)	CSA using D Latch(16 bits)
Delay(ns)	23.287	21.488
Power(mW)	650.42	650.51

The delay and device utilization required for the DCT implementation using conventional and Modified Wallace Multiplier is shown in Table IV.

TABLE IV
COMPARISON RESULT FOR DCT

Parameters	DCT using BEC	DCT using D Latch
Delay(ns)	328.22	308.14
Device Utilization	12045	12244

CONCLUSION

In this paper a modification to the Wallace multiplier is performed. The comparison result shows that the modified one reduces the number of half adders by 80%.
The introduction of carry select adder using D Latch in the final carry propagation path make the Wallace multiplier faster. The introduction of modified Wallace multiplier having CSA with D Latch in the final carry propagation path in DCT improved the performance of DCT in terms of delay and area.

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